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# Application Note

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# CableTest Technical Bulletin

## DC HiPot Description

The DC HiPot test is performed by applying a user-defined voltage to the Product Under Test (PUT) and by measuring the leakage current and monitoring for arc conditions...

*Synoptic:*

The DC HiPot test is performed by applying a user-defined voltage to the Product Under Test (PUT) and by measuring the leakage current and monitoring for arc conditions.

The test is facilitated by a high-voltage DC source that has a current limited output characteristic, as shown in Figure 1.

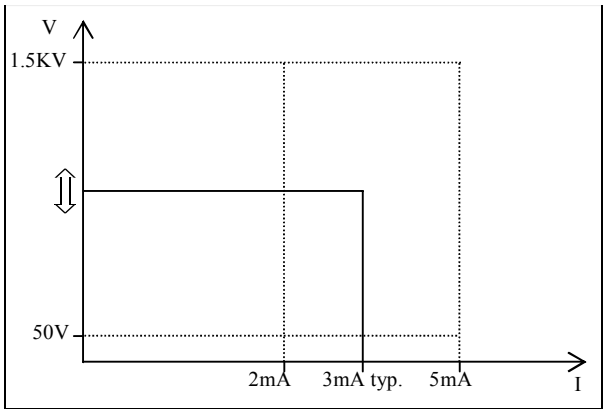


*Figure 1*

While the voltage is user programmable the current limit is factory set. During any time of the test the PUT will be inside the shaded area.

In the steady state mode this would be typically somewhere along the top horizontal side, which places the source in voltage compliance mode.

During the charging this would be along the right vertical side, which places the source in current compliance mode.

*Dynamic Characteristics:*

The dynamic characteristics of the DC Hi-Pot test have to do with the following elements:

1. The charging of the PUT's capacitance to the test voltage.
2. The dwell time.
3. The discharge of the PUT's capacitance to 0V.

These three elements can be identified in Figure 2 on the following page.

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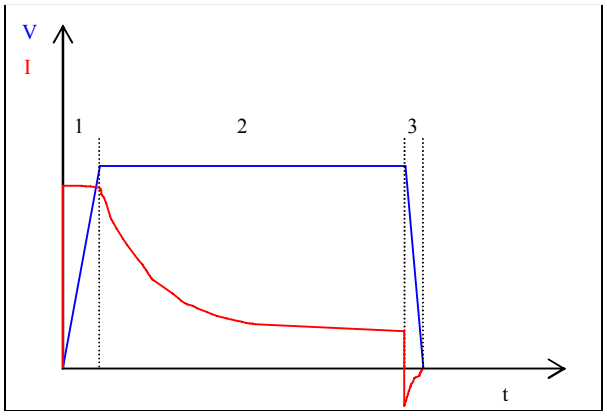


*Figure 2*

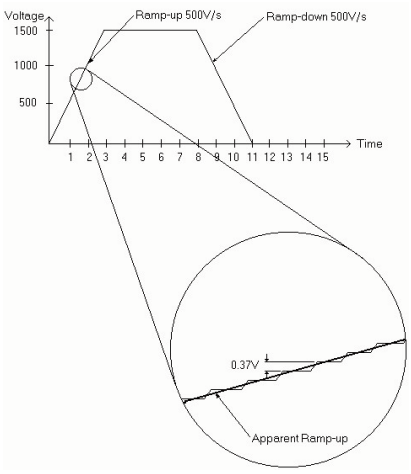


*Figure 3*

## *Charging Dynamics with no Ramp-Up:*

The charging of the PUT's capacitance to the test voltage takes place under constant current, as per the characteristics depicted in Figure 1.

The dynamics of the charging process are governed by equation 1 below.

$$\frac{dV}{dt} = \frac{I}{C} \qquad (1)$$

As an example, for a system stray capacitance of 1nF, a PUT capacitance of 600pF and a current limit of 2.5mA we obtain the following charging rate:

$$\frac{dV}{dt} \approx 1500 V/ms \qquad (2)$$

In the example above, it will take approximately 1/3 millisecond for the voltage to reach 500V. As the PUT capacitance increases, the voltage rate will decrease.

## *Charge Dynamics with Ramp-Up:*

When a user programmable ramp-up is specified, the charging takes place as in Figure 3. The ramping is performed via a series of micro-steps of approximately 0.37V each. The duration of each micro-step is automatically calculated based on the user-defined ramp-up rate.

The ramp rate between the micro-steps is also linear and is governed by the mechanism described under Charge Dynamics with no Ramp-Up.

## *Dwell Time Dynamics:*

Once the voltage on the PUT reaches the programmed limit, the DC source switches automatically in voltage compliance mode.

The dwell timer starts counting down only after the test voltage has been reached. In this mode, the current starts to decrease to the level sustained by the leakage in the PUT.

Depending on the dielectric material, a soaking effect might be observed. During the soaking, the leakage current decreases progressively to a steady state value. The higher initial value and the subsequent decrease can be attributed to the progressive saturation of the dielectric under an intense electrical field.

The leakage current is monitored (for a description of the several different modes that the system can be operated in, please refer to the Horizon 1500 User's Manual) and, at the end of the test is compared against the pass threshold.

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## *Discharge Dynamics with no Ramp-Down:*

After the dwell time has lapsed or after detecting certain error conditions (such as arcs, excessive leakage, palm switch etc.) a discharge cycle is initiated.

The discharge is performed by turning off the output of the DC high-voltage source and through a 10K resistor group to ground. The discharge is described by equation 3 below:

$$V = V_0 e^{-\frac{t}{\tau}} \qquad (3)$$

The discharge rate is not constant during the discharge as it follows an exponential law. The time needed to discharge the 1.6nF capacitance (system + DUT) from 500V to 1V is given in equation 4 and the equivalent discharge rate in equation 5:

$$t \approx 0.14ms \qquad (4)$$

$$\frac{dV}{dt} \approx 3570V/ms \qquad (5)$$

## *Discharge Dynamics with Ramp-Down:*

When a user programmable ramp-down is specified, the discharging takes place as in Figure 3.

The ramping is performed via a series of micro-steps of approximately 0.37V each. The duration of each micro-step is automatically calculated based on the user-defined ramp-down rate.

The ramp rate between the micro-steps is exponential and is governed by the mechanism described under Discharge Dynamics with no Ramp-Up.

*About CableTest Systems Inc.*

*CableTest Systems Inc. provides total cable testing solutions to a wide array of industries including aerospace, computers, medical, telecommunications, transportation and the military. Customers rely on CableTest's high voltage interconnect equipment to test their cables, wiring harnesses, power cords, and backplanes with speed, accuracy and reliability. You can learn more about CableTest Systems Inc. at www.CableTest.com.*

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